M-17
READ/WRITE MEMORY MODULES
FIELD SERVICE AND TRAINING MANUAL

SCOPE

The purpose of this manual is to describe the theory of operation of the M-17 family of read/write memory modules. These include the M-17-1-STD 2K core memory, the M-17-2-280 4K core memory, and the M-17-3-280 8K core memory.

Prior to using this manual, the reader should have knowledge of basic computer concepts and logical diagnostic techniques. In addition, the reader should be familiar with the operation of terminal-systems common port lines as described in *M-15 Terminal Control Unit* (MS-415) and *M-19-1-STD Terminal Clock* (MS-419).

CONTENTS

M-17-1, -2, and -3
READ/WRITE MEMORY MODULES

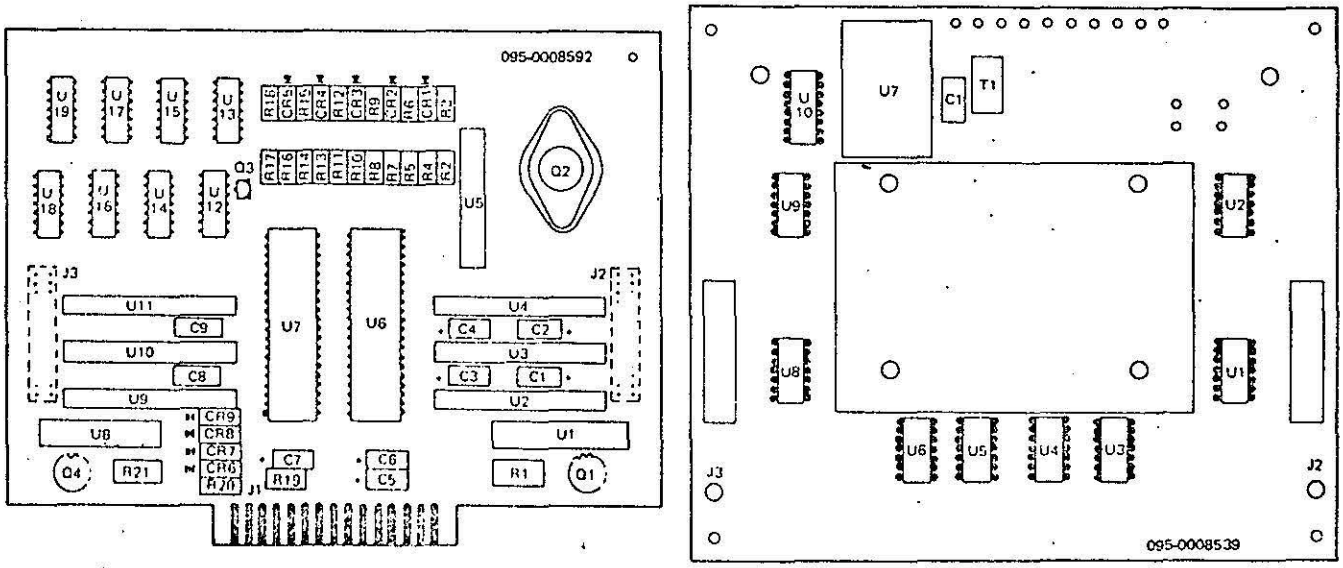

Fig. 1 M-17-1-STD memory module

INTRODUCTION

The terminal control unit module (TCU) contains a read-only memory to control the operation of the terminal. In some terminals, additional memory space is required to store program variables, tables, or totals. The additional memory space may be provided by an M-17 Read/Write Memory module.

There are three sizes of M-17 memory: 256 characters (M-17-1-STD), 512 characters (M-17-2-280), and 1024 characters (M-17-3-STD). Each bit of each eight-bit character is stored in a core. The time required to store (write) or retrieve (read) one bit is 7 μsec. and 56 μsec. is required for each character. The read/write timing of the memory is controlled by the clock module in the parent unit.

Control for the memory is provided by the TCU module. Control signals and data to be written are transferred to the memory module on the TCU common port lines. Memory status and the data read from memory are also transferred on the common port lines.

All M-17 memory modules consist of two printed circuit boards: a memory logic/driver board and a core array board. The two boards are physically connected by four spacers. Electrical connection between the boards is made through two 28-pin connectors.

The memory logic/driver board contains MOS/LSI arrays, integrated circuits, hybrid current sources and driver/grounders, and discrete components. The MOS/LSI arrays and integrated circuits provide function-code decode, address decode, and read/write timing. The hybrid current

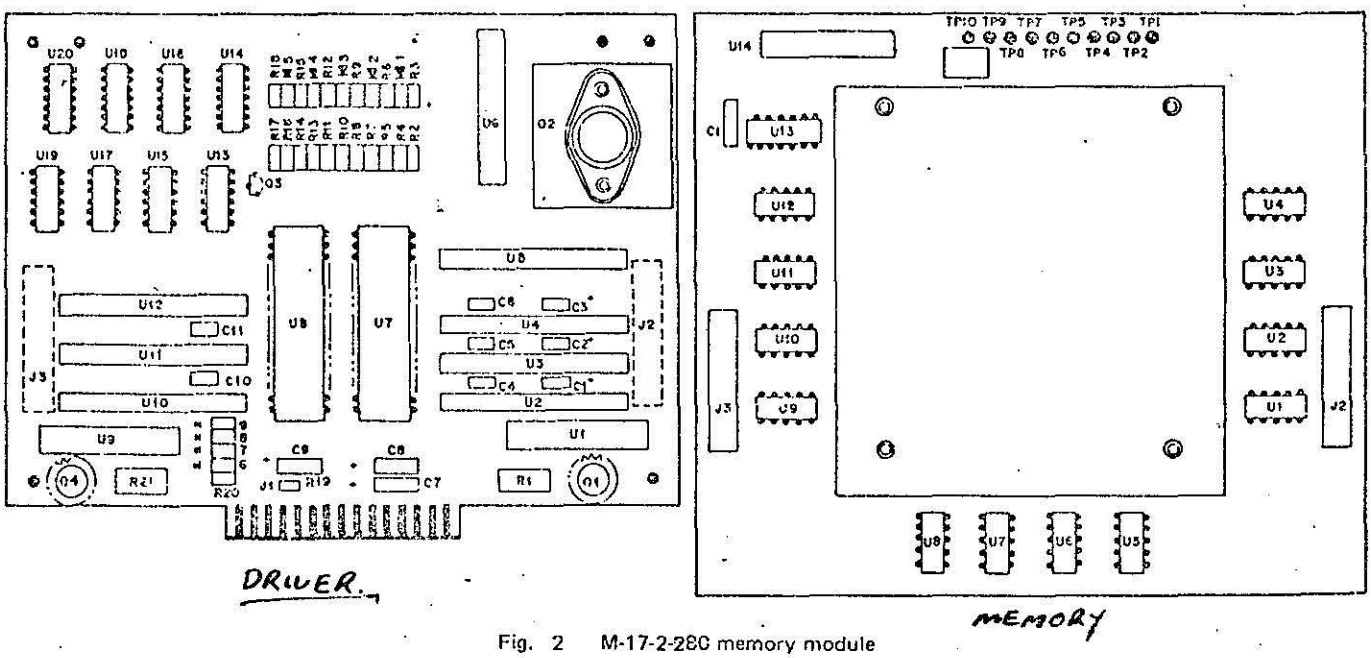

Fig. 2 M-17-2-280 memory module

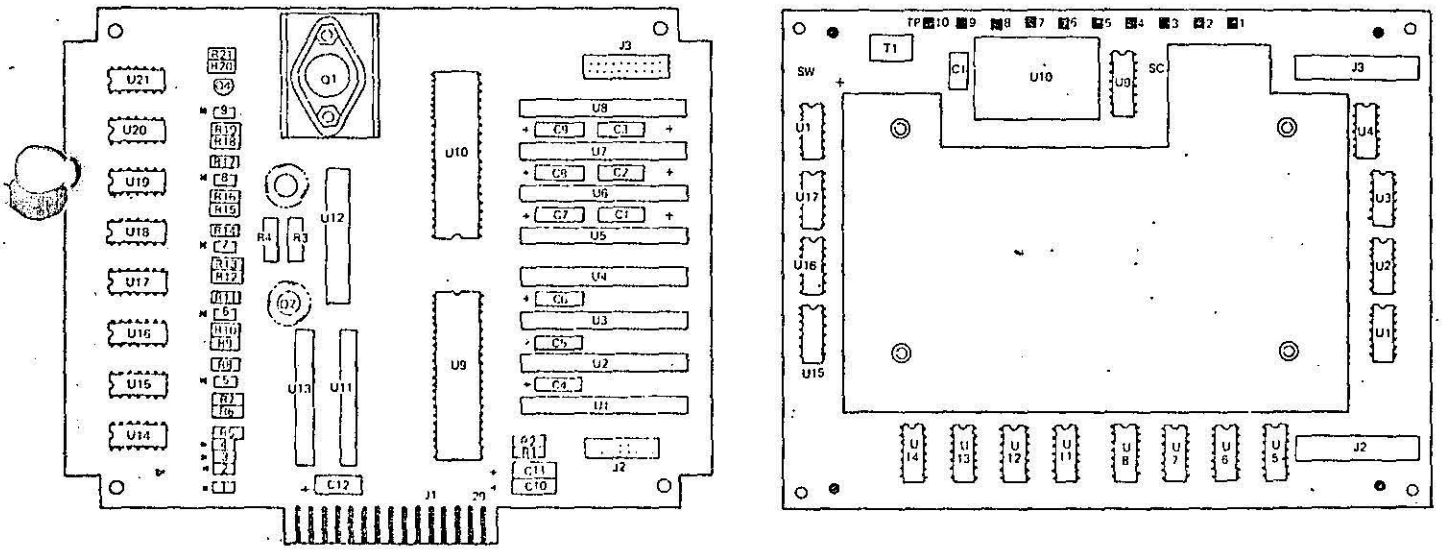

Fig. 3 M-17-3-STD memory module

sources provide regulated current for operation of the memory. The hybrid driver/grounders serve as switches for the regulated current. The discrete components on the board are used for decoupling the supply voltages, clamping the phase clocks, and converting voltage levels.

The core array board contains a lithium-core array, array isolation diodes, sense amplifiers, a strobe core, a pulse transformer, and a sense amplifier bias circuit.

The two boards of each memory are shown in figure 1 (256-character memory), figure 2 (512-character memory), and figure 3 (1024-character memory).

The electrical and environmental requirements for proper operation of the M-17 are listed below.

Voltage

+12 v.d.c. ±5 percent @ 1.2amp. peak
-12 v.d.c. ±5 percent @ 165ma. peak
-6.8 v.d.c. ±10 percent @ 10ma. peak

Temperature

Operating Range	32°F to 150°F
Storage Range	-40°F to 160°F

Relative Humidity

Operating Range	5 to 88 percent
Storage Range	5 to 88 percent

GENERAL DESCRIPTION

MEMORY OPERATION

The M-17 memory, like all core memories, stores data by magnetizing a core of magnetic material. Each core stores the state of one bit of digital information; for example, the M-17-2-280 memory has a capacity of 512 eight-bit characters for a total of 4096 cores.

As shown in figure 4, each donut-shaped core has three conductors through its center. Two of the three conductors, vertical drive and horizontal drive, have voltage applied to them by the memory-addressing circuitry. The sense wire has voltage induced into it when the magnetic state of the core changes.

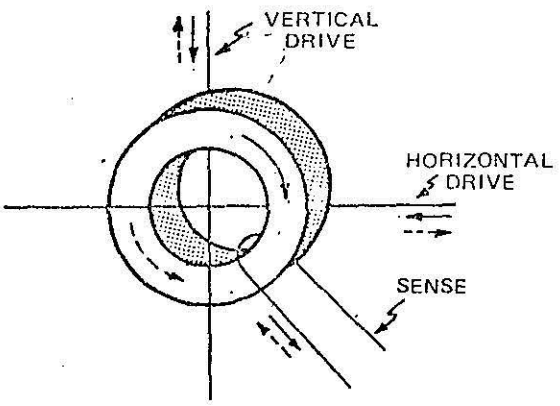

Fig. 4 Memory core

A core is magnetized by passing current through the horizontal drive line and the vertical drive line in the same direction. Each line carries only one half the current necessary to magnetize the core; this current is called half-select current. If there is half-select current in only one line or if the half-select current in both conductors is in opposite directions, the magnetic state of the core is not changed.

When a bit is written, the half-select currents in the horizontal drive line and vertical drive line flow in the same direction (solid arrows). Current in both lines is reversed (dashed arrows) to read the core. The direction the core is magnetized during the write operation is reversed during the read operation.

The decay and rise to the opposite polarity of the magnetic field during a read operation induces current into the sense

wire. A sense amplifier detects the induced voltage pulse. If a read operation is being performed, the output of the sense amplifier is transferred to the controlling device. The sense amplifier output is ignored during a write operation.

The M-17 core arrays are arranged in blocks of 256 eight-bit characters called sectors. The M-17-1-STD memory module has one sector, the M-17-2-280 has two sectors, and the M-17-3-STD has four sectors.

The contents of a two-bit register are used to determine from which of the four possible sectors a character is to be read or into which a character is to be written. This sector address register is loaded by the TCU.

An eight-bit binary character is transferred to the memory module from the TCU to select one of 256 character locations within the sector. The character is stored in an eight-bit character address register. The contents of this register can be incremented by one or transferred to the TCU when instructed to do so by the TCU.

The outputs from the registers and the bit position within the character are combined to provide the horizontal drive selection and vertical drive selection.

In addition to memory addressing logic and the core array, the M-17 memory modules contain control logic and data/status logic. These two logic groups are shown in relation to the memory addressing logic and core array in figure 5.

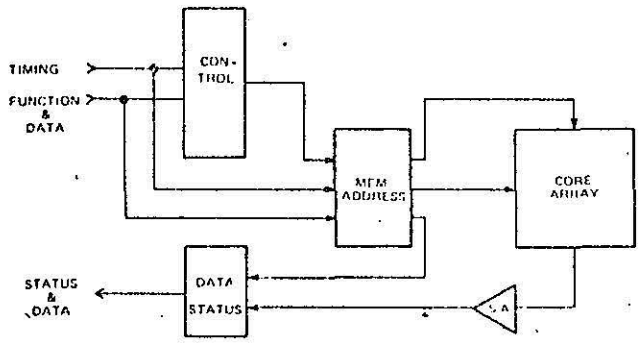

Fig. 5 Memory block diagram

The control logic decodes the function codes received from the TCU, initiates the read and write cycles, and controls the loading of the address registers. The data/status logic controls the transfer of status and data characters to the TCU.

All of the logic in the memory modules is designed to ensure that data can be stored in a specified location and then retrieved when needed by the TCU.

TCU-ISSUED FUNCTIONS

The M-17 read/write memory is operated as a module on a common port of the terminal control unit (TCU). The TCU controls the operation of the M-17 by issuing any of seven function codes. The codes are listed in table 1. Although eight function bits are transferred to the memory module, only the four most significant bits are decoded. The four least significant bits are ignored.

FUNCTION	b_8	b_7	b_6	b_5
Receive Sector Address	0	0	1	0
Receive Character Address	1	1	0	0
Present Character Address	1	0	1	0
Read Memory	1	0	0	0
Write Memory	0	1	0	0
Advance Character Address/ Read Memory	0	0	0	1
Advance Character Address/ Read Memory/Write Memory	0	1	0	1

Table 1. Memory function codes

RECEIVE SECTOR ADDRESS

M-17 memory core arrays are divided into sectors of 256 characters each. The M-17-1-STD has one sector, the M-17-2-280 has two sectors, and the M-17-3-STD has four sectors. A two-bit sector address register is used to store the sector address during execution of read and write functions.

The two least significant bits of the sector address character from the TCU are loaded into the sector address register a minimum of two character times after the module recognizes a receive sector address function code. During the two-character delay between receipt of the function code and the receipt of the address character, the address register is cleared. Refer to figure 6.

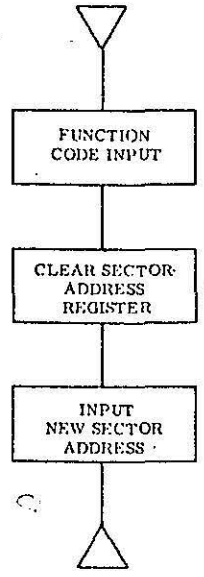

Fig. 6 Receive sector address

The four possible sector address characters and the minimum memory size required for use of each are given in table 2. Bits represented by X may be either ONE or ZERO.

Sector Address Characters								Minimum Memory Size
b_8	b_7	b_6	b_5	b_4	b_3	b_2	b_1	
X	X	X	X	X	X	0	0	2048 bits
X	X	X	X	X	X	0	1	4096 bits
X	X	X	X	X	X	1	0	8192 bits
X	X	X	X	X	X	1	1	8192 bits

Table 2 Sector address characters

The least significant bit (b_1) of the sector address character selects one of two groups of horizontal lines through the array. Bit b_2 selects one of two groups of vertical lines through the array. Refer to figure 7.

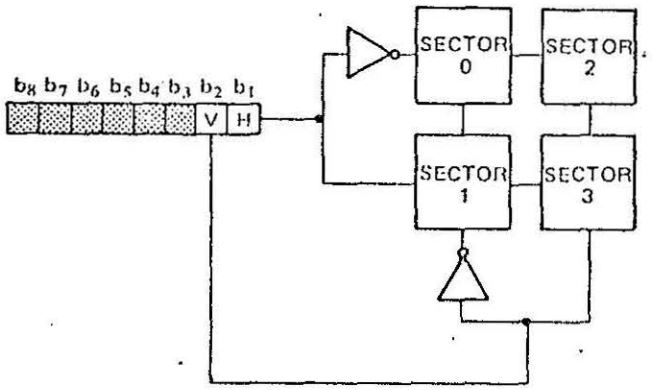

Fig. 7 Sector addressing

The contents of the sector address register can only be changed by the initial reset from the clock module or by receipt of a receive sector address function code.

RECEIVE CHARACTER ADDRESS

Recognition of the receive character address function code by the memory logic prepares the character address shift register to accept an eight-bit binary address character. A minimum of two character times after the memory logic recognizes the function code, one eight-bit character is transferred from the TCU. The character is shifted serially into the character address register and the previous character is shifted out. Refer to figure 8.

The binary content of the character address register selects one of 256 character locations in a specified sector to be read from or written into. The character address register contents remain unchanged until a subsequent receive character address function, an advance character address/read memory function, or an advance character address/read memory/write memory function is recognized. The character address register is cleared to address 000 after the parent unit is upsequenced.

PRESENT CHARACTER ADDRESS

The present character address function results in transferring the binary contents of the character address register to the TCU. The transfer is accomplished by recirculating the contents of the character address register.

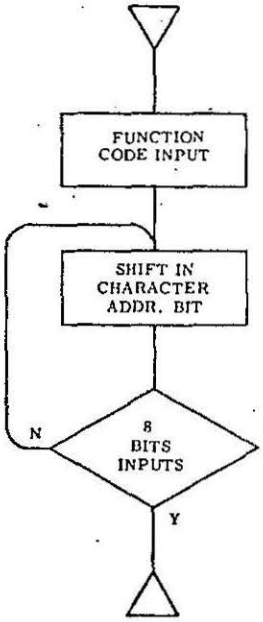

Fig. 8 Receive character address function

The memory logic delays transfer of the address until the second character time following receipt of the present character address function code. Refer to figure 9.

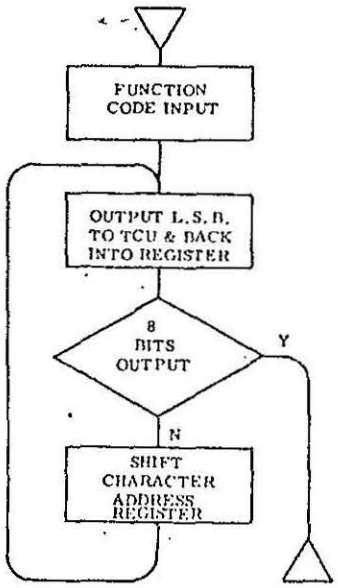

Fig. 9 Present character address function

Execution of the present character address function does not alter the contents of the character address register.

READ MEMORY

Recognition of a read memory function code causes the memory module to output one eight-bit character to the TCU. The address of the character transferred to the TCU is specified by the contents of the sector address register and the character address register.

The selected character is read during the second character time following receipt of the read function code. The

selected character is written back into the same location during the same 56 μsec. character time in which the character is read. Refer to figure 10.

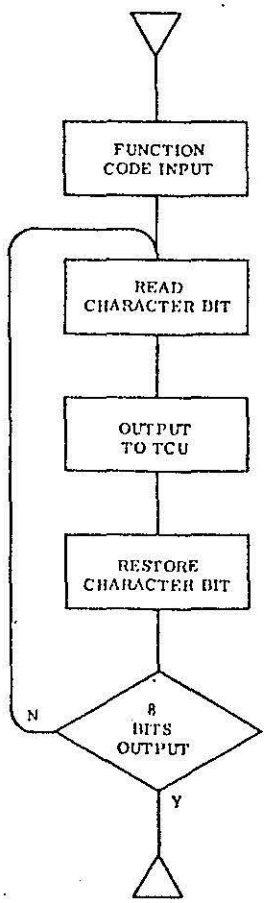

Fig. 10 Read memory function

Each character is read serially by bit, from the least significant bit (b_1) to the most significant bit (b_8). During each 7 μsec. bit time, one bit of the selected character is read, transferred to the TCU, and rewritten into the same memory core. This operation is referred to as a read/restore operation.

After performing a read memory function, the contents of the memory, the sector address register, and the character address register are the same as before performance of the function.

WRITE MEMORY

Receipt of the write memory function code conditions the memory logic to replace the contents of a prescribed character location with the next eight-bit data character transferred to the memory module.

A minimum of two character times (determined by TCU turnaround time) after sending the write memory function code, the TCU sends the character to be written. As each bit of the serially-transmitted character is received by the memory module, the selected character bit core is cleared by performing a read operation. During the same 7 μsec. bit time, the new bit is written into the core just cleared. This operation is referred to as a clear/write operation. Refer to figure 11.

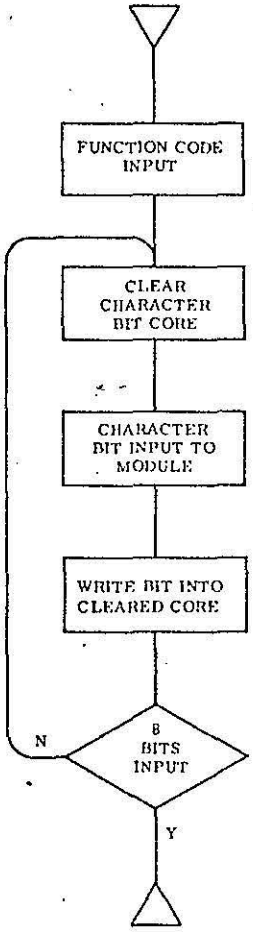

Fig. 11 Write memory function

The sector address register and the character address register are not changed by performing the write memory function. The selected memory location, after performing the function, contains the character received from the TCU.

ADVANCE CHARACTER ADDRESS/ READ MEMORY

After receiving an advance character address/read memory function, the memory module logic increments the contents of the character address register by one and then reads the character from the new address.

The sector address register is unaffected when incrementing the character address register. If the character address register is advanced from 255 to 000, the sector address register is not altered. Refer to figure 12.

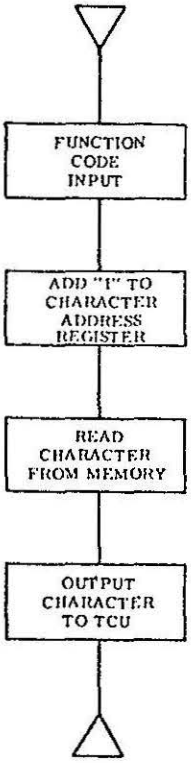

Fig. 12 Advance character address/read memory function

After the character address is incremented, the contents of the new location are read and transferred to the TCU. The actual read operation and timing are identical to that of the read memory function.

ADVANCE CHARACTER ADDRESS/READ MEMORY/WRITE MEMORY

Upon receiving an advance character address/read memory/write memory function code, the read/write memory module logic increments the character address register contents by one. The content of the core location specified by the new address is read and transferred to the TCU. The next data character transferred to the memory module is written into the location specified by the incremented character address register. Refer to figure 13.

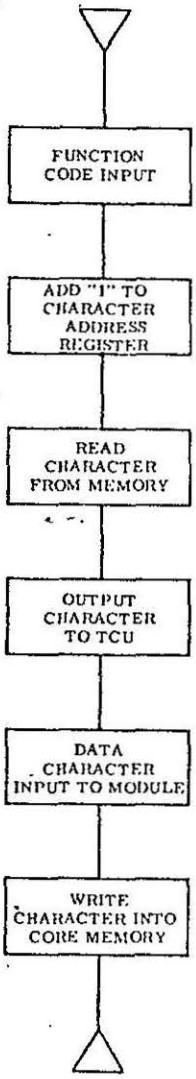

Fig. 13 Advance character address/read memory/write memory function

The read and write operations are performed as described previously. The data transferred to the TCU during the read memory portion of this function is sometimes ignored by the firmware program. This makes the advance character address/read memory/write memory function effectively an advance character address/write memory function.

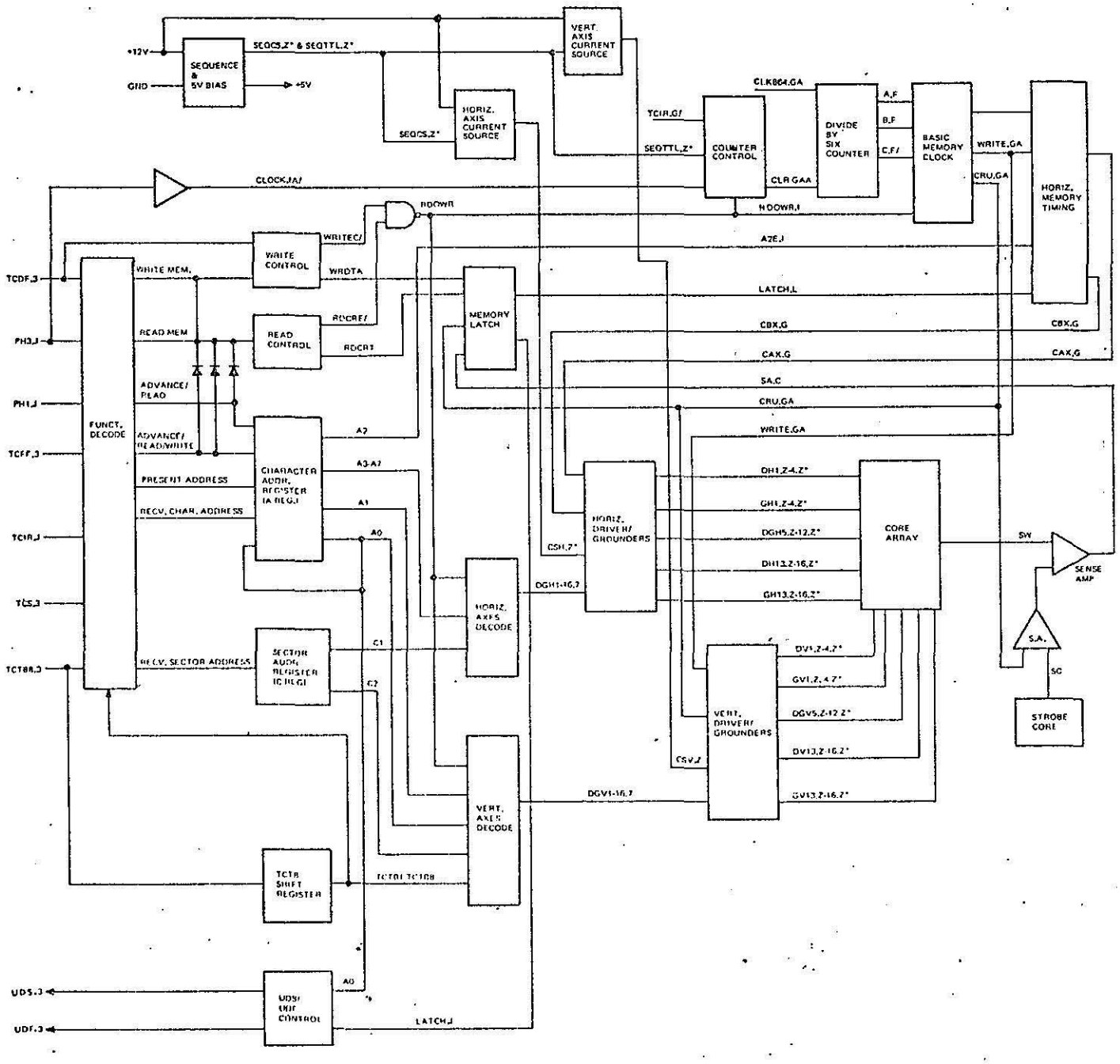

Fig. 14 - Read/write memory block diagram

LOGIC DESCRIPTION

The circuitry composing the M-17 read/write memory module can be divided into a number of logical segments. These segments, shown in the block diagram figure 14, can consist of one logic circuit or many circuits.

As the unit containing the memory module is turned ON, the power supply voltages rise at random. To ensure that the contents of the memory are not lost, the +12 v. is monitored. The horizontal and vertical axis current sources are inhibited until the +12 v. has reached +9 v. The +5 v. for the memory TTL logic is supplied by the +12 v.d.c. The counter used to generate the bit read and bit write timing is also inhibited until the parent unit is completely upsequenced.

After upsequencing, the memory module is in an idle condition until the TCU specifies the memory sector which data is to be read from or written into. The address contained in the character address register and the sector address register is decoded when a read or write function is issued.

Regardless whether a read function or write function is issued, the address is decoded in the same way. The horizontal axis decode selects a string of cores containing the eight bits of the desired character. The vertical axis decode sequentially selects each bit of the desired character.

The same sequence is followed for each bit read or written. In the first half of each 7 μsec. bit time, the selected bit is

read and cleared. In the last half of the bit time, the contents of the memory latch is written into the selected bit position.

The difference between a read function and write function is the input to the memory. In a read function, the memory latch is loaded with the bit read during the first half of the bit time. This bit is output to the TCU, and during the second half of the bit time, the content of the memory latch is written into the same memory location from which it has been read. The memory latch contains a bit from the TCU during the second half of a write function bit time. During the first half of the bit time, the selected core is cleared. The bit in the memory latch is written into the selected core during the second half of the bit time.

The following descriptions of each segment elaborate on the operation of each logical segment.

SEQUENCE AND +5 V BIAS

To prevent destroying the contents of memory while upsequencing and downsequencing the parent unit, the memory module is provided with a sequence control. Included in the same hybrid circuit pack with the sequence control is a +5 v. bias supply.

The sequence control circuitry provides a control signal for the horizontal axis and vertical axis current sources. A control signal is also provided for the counter control logic. The circuitry ensures that the current sources are inoperative until the +12 v. power supply output has reached approximately +9 v. The control signal for the current sources is SEQCS.Z*. SEQTTL.Z* is the control signal for the counter control logic.

As the output of the +12 v. supply rises toward its nominal voltage, the SEQCS.Z* and SEQTTL.Z* outputs change state. SEQCS.Z* rises as the input voltage rises until the input voltage reaches approximately +9 v. When the input voltage reaches +9 v., SEQCS.Z* (at +1.7 v.) switches to ground to activate the current sources. At the time that SEQCS.Z* switches from +1.7 v. to 0 v., SEQTTL.Z* changes from 0 v. to +5 v. to permit the counter control logic to become operational. Refer to figure 15 for sequence control timing.

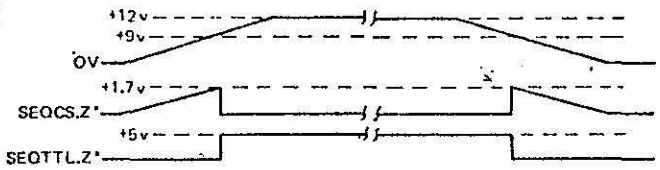

Fig. 15 Sequence control timing

When the input voltage drops below +9 v., SEQCS.Z* and SEQTTL.Z* change state to inhibit the operation of the current sources and the counter control logic. This characteristic of the circuitry ensures that the data stored in the core array is not destroyed during downsequence.

The +5v. bias voltage supply is derived from the +12v. input voltage to the hybrid circuit. A zener-controlled voltage regulator maintains the output voltage at +5v. The bias voltage is used to operate the various TTL integrated circuits and hybrid circuits on both the logic board and the core array board of the memory module.

HORIZONTAL AXIS CURRENT SOURCE

The horizontal axis current source regulates the current path to ground for the selected horizontal axis line of the core array. The +12 v. for the opposite end of the selected horizontal axis line is provided through one of the horizontal drivers. Refer to figure 16.

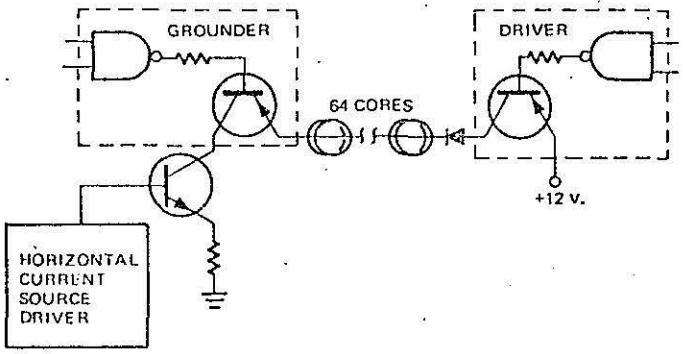

Fig. 16 Horizontal axis current path

The current drawn through a selected horizontal axis line (approximately 320ma.) is the half-select current for the core to be read or written.

The current source is operational when the term SEQCS.Z* is at ground indicating that the output of the +12 v. power supply is at least +9 v.

VERTICAL AXIS CURRENT SOURCE

The vertical axis current source regulates the current path to ground for the selected vertical axis line of the core array. The +12 v. for the opposite end of the selected vertical line is provided through one of the vertical axis drivers. Refer to figure 17.

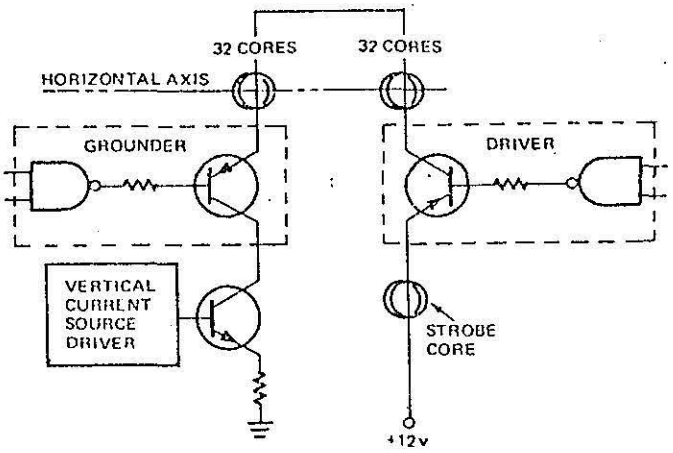

Fig. 17 Vertical axis current path

The current drawn through the selected vertical axis line (approximately 320ma.) is the half-select current for the core to be read or written.

The vertical axis current source is operational when the term SEQCS.Z* is at ground indicating that the output of the +12 v. power supply is at least +9 v.

COUNTER CONTROL

The counter control logic comprises a power sequence flip-flop and an AND gate. The power sequence flip-flop, CLEAR.F, inhibits the operation of the divide-by-six counter until the +12 v. power supply output has reached at least +9 v. (SEQTTL.Z* High), and the initial reset line (TCIR.G/) has switched High. After the parent unit has properly upsequenced (CLEAR.F set), control of the counter control logic is the responsibility of RDOWR.IAA. RDOWR.IAA is High when either a read operation or a write operation is initiated. CLEAR.F and RDOWR.IAA are anded to generate the counter control term CLR.GAA. Refer to figure 18 for the counter control logic timing.

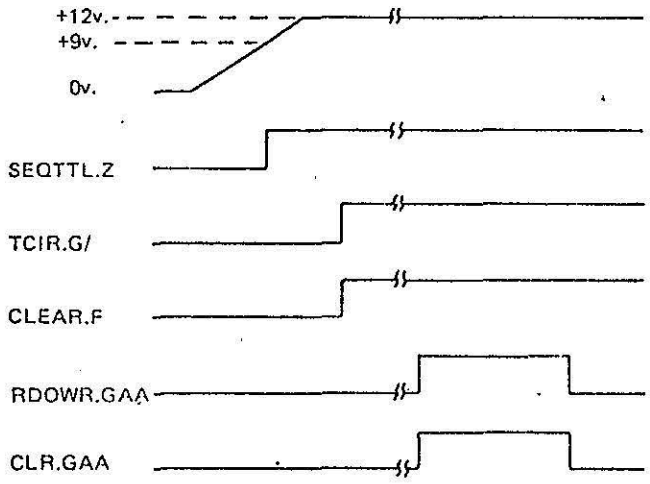

Fig. 18 Counter control logic timing

CLR.GAA is High for the 56 μsec. duration of RDOWR.IAA. After a character is read or written and RDOWR.IAA switches Low, CLR.GAA goes Low to reset the divide-by-six counter flip-flops.

DIVIDE-BY-SIX COUNTER

The divide-by-six counter divides the 7 μsec. of each bit time into six equal parts. The output of the counter, shown in figure 19, is used by the M-17 module to generate the basic memory clock terms.

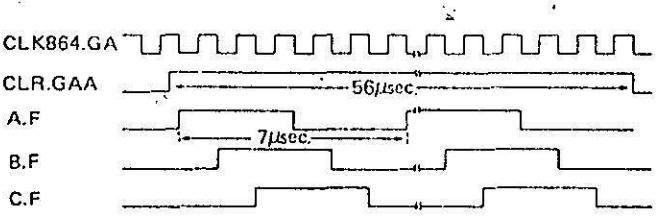

Fig. 19 Divide-by-six counter timing

This three flip-flop counter is inhibited from counting until the counter control term CLR.GAA is High. With CLR.GAA High, the counter is permitted to change state with each negative excursion of CLK864.GA. The excursions occur every 1.157 μsec. or six times for each 7 μsec. bit time. The counter continues to run for the 56 μsec. duration of RDOWR.IAA. The three flip-flops are reset when RDOWR.IAA goes Low.

FUNCTION DECODE

The memory module logic recognizes seven function codes: receive sector address, receive character address, present address, read memory, write memory, advance character address/read memory, and advance character address/read memory/write memory.

The terminal control unit sends the eight-bit function code to the M-17 memory module on TCDF.3. To identify the function code character as the function code for the memory module, TCFF.3 and TCS.3 are Low with the function code character. The function flag, TCFF.3 Low, indicates that the character on TCDF.3 is a function character as opposed to a data character. TCDF.3 and TCFF.3 are output to all modules and units on the common port, but TCS.3 is unique to the memory module.

TCS.3, terminal strobe, selects the memory module as the module to accept the character on TCDF.3.

The function code is transmitted as an eight-bit serial character. The least significant four bits are ignored. Bits b_5 through b_8 contain the function code. The bit configuration for the various codes are shown in table 1.

Receipt of the receive sector address function code (0010XXXX) conditions the sector address register, C register, to accept a two-bit sector address. The sector address is used in the memory address decode to determine which one of four 2048-bit sectors contains the desired character.

The binary address of the desired character within a sector is stored in the character address register. The character address register, A register, is loaded with an eight-bit address character received after recognizing a receive character address function code (1100XXXX).

Recognition of a read memory function code (1000XXXX) causes the memory module to read the eight-bit contents of the location designated by the A register from the memory sector designated by the C register. The character is then transmitted to the TCU on UDS.3.

The character transmitted to the memory module after a write memory function code (0100XXXX) is written into the memory location designated by the contents of the A-register and C-register.

A function code with bit b_5 Low causes the memory module logic to increment the A-register contents by one. After incrementing the A-register contents, the character location specified by the incremented A register is read and transferred to the TCU. If the function code is 0101XXXX, the character transmitted to the memory module after the read operation is written into the location specified by the incremented A-register. If the function code is 0001XXXX, the function is completed after reading the desired memory location.

In order for the TCU program to determine the address contained in the A register, the TCU outputs a present address function code (1010XXXX) to the memory module. The memory module responds to this function by transferring the contents of the A register to the TCU on UDS.3.

UDS/UDF CONTROL

The UDS/UDF control logic directs the transfer of data and status to the TCU. The data and status characters are transferred to the TCU on UDS.3. To distinguish between data and status, the data flag line (UDF.3) is Low when transmitting data and High when transmitting status.

A ready status code (0001XXXX) is constantly transmitted to the TCU when no data is being transferred from the memory module. When a character is being read from core, the character is transmitted serially by bit on UDS.3. The contents of the A register are also transmitted serially by bit on UDS.3 when a present address function is performed.

TCTB SHIFT REGISTER

The timing required to transfer characters to and from the memory module is provided by the TCTB shift register. This register is initiated when TCTB8.3 from the TCU goes low. A string of seven 7-μsec. Low pulses are generated as a result of TCTB8.3 going Low. Refer to figure 20.

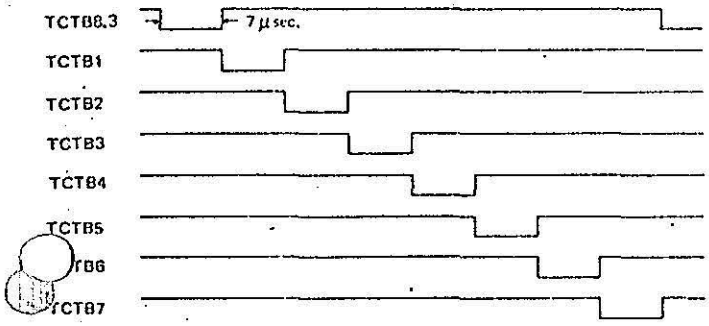

Fig. 20 TCTB timing

The timing pulses generated by the shift register are used by the function decode logic. The pulses provide a means of determining which bit is a logic ONE on the TCDF.3 line. The state of the TCDF.3 line is examined at each TCTB time, and when an equal comparison is made, a logic ONE bit is recorded. For example, if TCDF.3 is Low at TCTB6 time, bit 6 of the received character is considered as a logic ONE.

The timing pulses are also used in the character address decode for the bit timing. Characters are read and written serially by bit. The bit being read or written at any given time during a read or write operation is determined by the TCTB timing pulses.

SECTOR ADDRESS REGISTER

The sector address register (C register) is a two-bit register used to store the address of the memory sector being read from or written to. This register is loaded with the two least significant bits of the eight-bit character received following recognition of a receive sector address function. The two C-register bits address one of four 256-character (2048 bit) sectors.

The state of the least significant bit of the C register, C1, is monitored by the horizontal axis decoded logic. C2, the most significant bit of the register, is used by the vertical axis decode.

The state of the C register can only be altered by generation of TCIR.J or by execution of a receive sector address function.

CHARACTER ADDRESS REGISTER

The character address register (A register) is an eight-bit shift register used to store the binary character address. With the eight-bit address, it is possible to access any of the 256 characters in a sector. The eight-bit contents of the A-register can be altered by execution of a receive character address function or by one of the two advance character address functions.

During a receive character address function, the bits of the character address are shifted one bit at a time from the most significant bit position (A_7) to the least significant bit position (A_0).

When performing either advance character address function, one is added to the least significant bit. The contents of the register are shifted one position to the right and the result of the addition is stored in A_7. If a carry occurs as a result of the addition, one is again added to the least significant bit and the result is shifted into A_7. One is added to the least significant bit and the result stored in position A_7 until no carry is generated or until the register contents have been shifted eight times. If no carry is generated, the content of A_0 is shifted into A_7 until eight shifts occur. Refer to the bubble flow in figure 21.

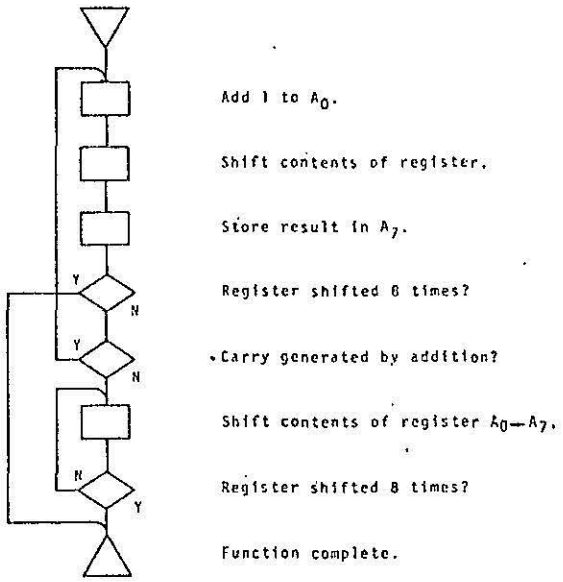

Fig. 21 Advance character address sequence

In performing a present address function, the contents of the least significant bit position (A_0) is output on UDS.3 and shifted into A_7. The shifting and transferring of bits from A_0 continues until eight bits have been transferred, and the A register has returned to its original state.

The contents of A_0 and A_1 are used in the vertical axis decode. A_2 is used in the horizontal memory timing to select the matrix. Logic bits A_3 through A_7 are used in the horizontal axis decode. Refer to figure 22 for a functional diagram of the A register.

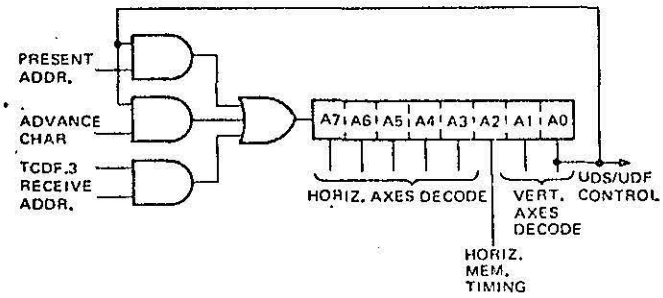

Fig. 22 A-register functional diagram

READ CONTROL

The read control logic generates the logic term necessary to properly perform a read operation. The inputs to the read control logic are provided when the function decode logic recognizes a read memory function or one of the two advance character address/read memory functions.

Two major terms are generated by the read control logic: RDCRE/ and RDCRT. RDCRE/ is used in the generation of the general read or write control term RDOWR. RDCRT gates the output of the memory sense amplifier into the memory latch. RDOWR, when Low, activates the horizontal and vertical axis decode and permits the basic memory clock terms to be generated.

The timing involved in recognizing a read function and performing the read function is shown in figure 23. After recognizing that a read function is to be performed, the memory module logic delays six bit times before starting the read. The delay is necessary to permit transmission of the character bits to be synchronized with TCTB1 through TCTB8.

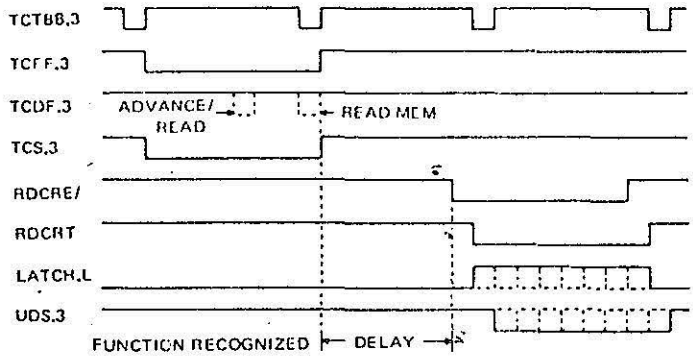

Fig. 23 Read control timing

In order to output each bit of the selected character location at its respective bit time (for example, bit 1 at TCTB1 time), the M-17 addressing logic is activated two bit times (14 μsec) before the bit is transferred to the TCU on the UDS.3 line. One bit time is required to address and read the selected bit and another bit time to transfer the bit from the memory latch to the UDS.3 logic.

RDCRE/ is Low at TCTB7 to permit setting RDOWR to activate the basic memory clock and the axis decode. One bit time later (TCTB8), RDCRT is Low to permit setting of the memory latch, LATCH.L, when a ONE bit is detected.

At TCTB1 time, the bit read at TCTB8 time is output to the TCU on UDS.3. The bit read at TCTB1 time is output at TCTB2. The cycle continues until the eighth bit of the selected character (read at TCTB7 time) is transferred to the TCU at TCTB8 time.

WRITE CONTROL

The write control logic directs the operation of the memory module during a write operation. Two major terms (WRITEC/ and WRDTA) are generated as a result of recognizing a write memory function code and receiving the character to be written.

WRITEC/, like RDCRE/ in the read control logic, is used to generate RDOWR for the axis decode and the basic memory clock. WRDTA, write data, is used to control the memory latch during a write operation. WRDTA varies with the character bits on TCDF.3. Figure 24 shows the timing involved in a write operation.

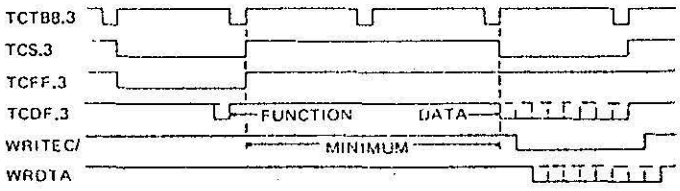

Fig. 24 Write control timing

A minimum of two character times after the write memory function code is recognized, the character to be written is received from the TCU. The two character time minimum is determined by the turnaround time of the TCU. The TCU is unable to output a function code character and then output a data character in less than four character times, although the memory module logic can react faster.

One bit time after the TCU transfers the first bit of the data character to the memory module, WRITEC/ generates RDOWR. The data bits on WRDTA are input to the memory latch starting one bit time after WRITEC/. Bits are written into core as a result of setting the memory latch. The two bit delay is a result of the MOS/LSI logic propogation time.

MEMORY LATCH

The memory latch, shown schematically in figure 25, is used for temporary storage of the bit read during a read operation or the bit to be written during a write operation. The latch is reset after the state of latch is examined by the memory module logic.

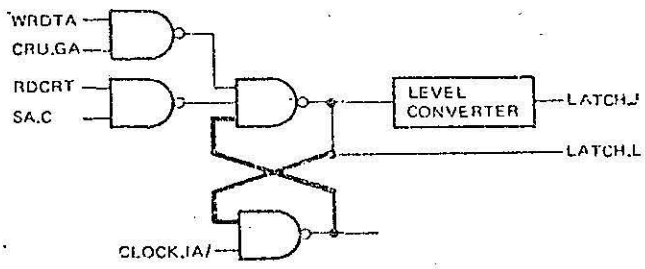

Fig. 25 Memory latch schematic

During the read operation, the latch is set when a ONE bit is detected by the memory sense amplifier, SA.C. The latch output is sampled by the UDS/UDF control logic for data transfer to the TCU and by the horizontal memory timing logic to permit restoring the core read to its preread state. After the memory latch output is sampled, the latch is reset by CLOCK.IA/ (PH3.J at TTL logic levels).

The latch is set during a write operation when a ONE bit is to be written in memory (WRDTA High). The output of the latch is monitored by the horizontal memory timing logic. The horizontal memory timing logic controls writing of bits in the core array.

HORIZONTAL AXIS DECODE

The horizontal axis decode logic provides 16 address inputs (DGH1 through 16) for the hybrid horizontal driver/grounders. Of the 16 possible inputs, only two are generated for any given character and sector address.

Bit A_3 through A_7 of the character address register (A register) and bit C_1 of the sector address register (C register) are used in the horizontal axis decode. Table 3 shows the 16 DGH1.7 through DGH16.7 lines and the A-register and C-register configurations for each line.

The timing for DGH1-16.7 is provided by RDOWR. The decode of the A-register and C-register configurations does not occur until the read or write term, RDOWR, is Low.

DGH1.7 = A_4' A_3' C_1'

DGH2.7 = A_4' A_3 C_1'

DGH3.7 = A_4 A_3' C_1'

DGH4.7 = A_4 A_3 C_1'

DGH5.7 = A_7' A_6' A_5'

DGH6.7 = A_7' A_6' A_5

DGH7.7 = A_7' A_6 A_5'

DGH8.7 = A_7' A_6 A_5

DGH9.7 = A_7 A_6' A_5'

DGH10.7 = A_7 A_6' A_5

DGH11.7 = A_7 A_6 A_5'

DGH12.7 = A_7 A_6 A_5

DGH13.7 = A_4' A_3' C_1

DGH14.7 = A_4' A_3 C_1

DGH15.7 = A_4 A_3' C_1

DGH16.7 = A_4 A_3 C_1

DGH13 through 16.7 are only used with memories larger than 2048 bits.

Table 3 Horizontal axis decode lines

VERTICAL AXIS DECODE

The vertical axis decode logic provides 16 inputs to the hybrid vertical driver/grounders. Of the 16 possible inputs, (DGV1.7 through DGV16.7), only two are generated for any given combinations of the A-register output, the C-register output, and the TCTB shift register output. Table 4 lists the DGV1.7 through DGV16.7 lines and the character address, sector address, and timing bit configurations for each line.

The timing for DGV1.7 through DGV4.7 and DGV13.7 through DGV16.7 is provided by RDOWR. DGV5.7 through DGV12.7 are gated by a read term or a write term occurring at the same time that RDOWR is generated. The TCTB inputs to the decode logic are used for bit read and write timing.

BASIC MEMORY CLOCK

The basic memory clock logic generates the read and write timing for the memory. The three clock terms (READ.GA, CRU.GA, and WRITE.GA) are generated by this logic for each bit read or written. These terms are a decode of the divide-by-six counter output (A.F, B.F and C.F) gates with RDOWR. Figure 26 shows the timing involved in the basic memory clock logic.

READ.GA is used in generating the horizontal memory timing pulses CAX.G and CBX.G. CRU.GA is used to gate

DGV1.7 = A_1' A_0' C_2'

DGV2.7 = A_1' A_0 C_2'

DGV3.7 = A_1 A_0' C_2'

DGV4.7 = A_1 A_0 C_2'

DGV5.7 = TCTB7 RDCRE + TCTB2 WRITEC

DGV6.7 = TCTB8 RDCRE + TCTB3 WRITEC

DGV7.7 = TCTB1 RDCRE + TCTB4 WRITEC

DGV8.7 = TCTB2 RDCRE + TCTB5 WRITEC

DGV9.7 = TCTB3 RDCRE + TCTB6 WRITEC

DGV10.7 = TCTB4 RDCRE + TCTB7 WRITEC

DGV11.7 = TCTB5 RDCRE + TCTB8 WRITEC

DGV12.7 = TCTB6 RDCRE + TCTB1 WRITEC

DGV13.7 = A_1' A_0' C_2

DGV14.7 = A_1' A_0 C_2

DGV15.7 = A_1 A_0' C_2

DGV16.7 = A_1 A_0 C_2

DGV13 through 16.7 are only used with memories larger than 4096 bits.

Table 4 Vertical axis decode lines

the vertical driver/grounders during the read cycle of a read/restore operation and during the clear cycle of a clear/write operation. CRU.GA also serves as the gating window for the memory sense amplifier and as the gating term for character bit input during a write operation. WRITE.GA provides timing for both the horizontal memory timing logic and the vertical driver/grounders.

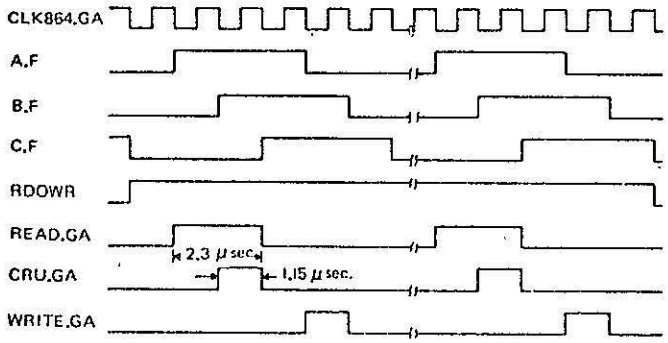

Fig. 26 Basic memory clock timing

HORIZONTAL MEMORY TIMING

The horizontal memory timing logic controls the timing and direction of current flow in the horizontal axis lines. The terms generated by the horizontal memory timing logic are CAX.G and CBX.G.

The timing for CAX.G and CBX.G is provided by READ.GA and WRITE.GA from the basic memory clock logic. The state of bit A_2 of the character address register, A2E.I, determines which of the two terms is output during the read portion of a read/restore operation or during the write portion of a clear/write operation.

The core arrays in all M-17 memories are divided into two matrices. By controlling the state of CAX.G and CBX.G, A2E.I determines which of the matrices contains the selected character.

The state of the memory latch, LATCH.L, is also gated with WRITE.GA and A2E.I during the restore portion of a read/restore operation or the write portion of a clear/write operation. The equations and timing for CAX.G and CBX.G are shown in figure 27.

CAX.G = READ.GA · A2E.I + WRITE.GA · A2E.I/ · LATCH.L

CBX.G = READ.GA · A2E.I/ + WRITE.GA · A2E.I/ · LATCH.L

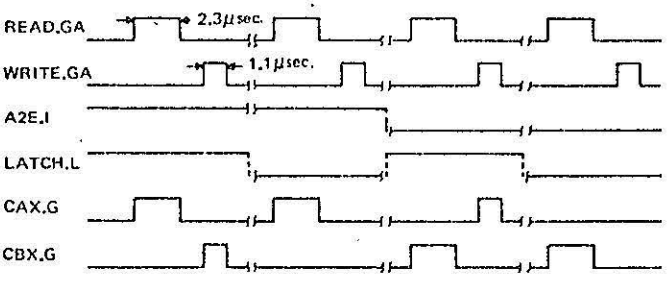

Fig. 27 Horizontal memory timing

Figure 27 shows the various configurations of CAX.G and CBX.G. The timing between each break in the timing diagram represents one bit time. The timing diagram is not intended to depict four bits in the same character since the state of A2E.I cannot change while performing either a read function or a write function on a given character location.

HORIZONTAL DRIVER/GROUNDERS

The horizontal driver/grounder circuits control the half-select current drawn through the horizontal axis lines. The inputs to the hybrid horizontal driver/grounders (DGH1-16.7, CAX.G, and CBX.G) activate two lines of the 24 output lines to the core array. One of the two lines provides +12 v. for the selected horizontal lines, and the other activated line provides the current path to ground through the horizontal axis current source. Figure 28 shows the operation of the horizontal driver/grounders for the character in location 000 in a 2K M-17.

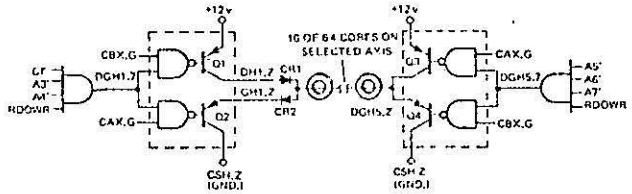

Fig. 28 Horizontal driver/grounders

In figure 28, the five most significant bits of the character address and the least significant bit of sector address are decoded by the horizontal axis decode logic. With an address of sector 00 and character 000, DGH1.7 and DGH5.7 are generated. DGH1.7 and DGH5.7 are combined with CAX.G or CBX.G to activate one driver circuit and one grounder circuit. With A2E.I Low, CBX.G is High during the read or clear portion of a character read or character write operation, and CAX.G is High during the restore or write portion of this operation.

During the read portion of the operation, driver transistor Q1 and grounder transistor Q4 are turned ON. In the illustration, current flows from left to right through the selected string of 64 cores. If a bit is to be written, transistors Q2 and Q3 are ON during the write portion of the operation to reverse the direction of current in the selected core string.

In the 2048 bit version of the M-17 read/write memory module, 16 of the possible 24 horizontal driver/grounder lines are used. Memories larger than 2048 bits require the entire 24 lines.

VERTICAL DRIVER/GROUNDERS

The vertical driver/grounder circuits control the half-select current drawn through the vertical or folded axis lines. Two outputs of a possible 24 are activated for any given configuration of A_0, A_1, C_2 (DGV1.7 through DGV4.7 and DGV13.7 through DGV16.7), and the bit position to be read or written (DGV5.7 through 12.7). One output of the two provides +12 v. for the selected vertical axis. The other activated output completes the current path for the selected vertical axis line to ground. Figure 29 shows the operation of the vertical driver/grounders for bit 1 of the character in location 000 of a 2K or 4K memory.

In the illustration, the two least significant bits of the character address and the most significant bit of the sector

address are decoded by the vertical axis decode logic. The vertical axis decode logic also selects the bit position in the character to be read or written. Selecting the first bit of character 000 generates DGV1.7 and DGV5.7. DGV1.7 and DGV5.7 are gated with the memory timing terms CRU.GA and WRITE.GA. During the read portion of a memory operation, transistors Q5 and Q8 are turned ON to select a vertical string of 64 cores. The current flows from left to right in the illustration. The direction of current flow is reversed during the write portion of the memory operation by turning ON transistors Q6 and Q7.

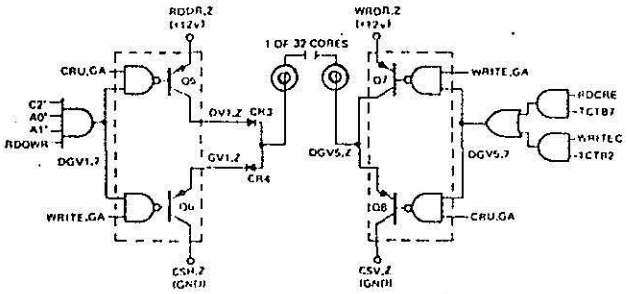

Fig. 29 Vertical driver/grounders

Memories having 2048 and 4096 bits capacity require only 16 of the 24 vertical driver/grounder outputs. The 8192 bit memories require the entire 24 outputs for proper addressing.

CORE ARRAY

The core array is the segment of the read/write memory module in which data is stored. The storage is accomplished through the use of donut-shaped lithium cores. Each core is capable of storing one bit.

Figure 30 depicts the physical arrangement of the core array. The total number of cores in the memory are divided into two equal groups or matrices. Each matrix comprises one (M-17-1-STD), two (M-17-2-280), or four (M-17-3-STD) groups of 1024 cores. The matrix containing the desired character is selected by the state of bit A_2 in the character address register. The group of 1024 cores containing the desired character within a matrix is selected by decoding the two-bit contents of the sector address register. To select the horizontal string of cores (1 of 32) within the sector, the five most significant bits of the character address register are decoded. A decode of the bit position within a character and the two least significant bits of the character address register are used to select the vertical string of cores (1 of 32).

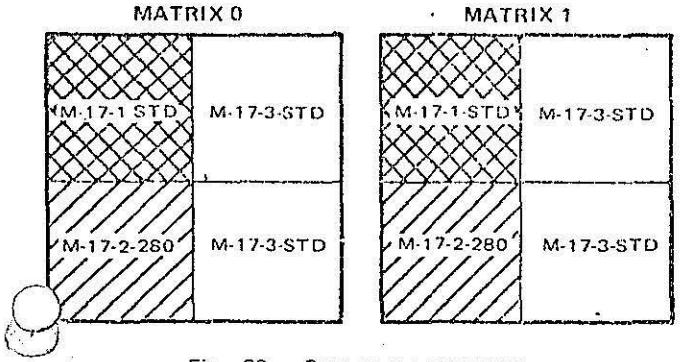

Fig. 30 Core array arrangement

The core arrangement for a 2048-bit memory (M-17-1-STD) is shown in figure 31. The horizontal axis lines run through both matrices. Each vertical axis line runs through one core on each horizontal line in a matrix. The same vertical axis line is folded over and runs through another core on each of the horizontal lines in the other matrix.

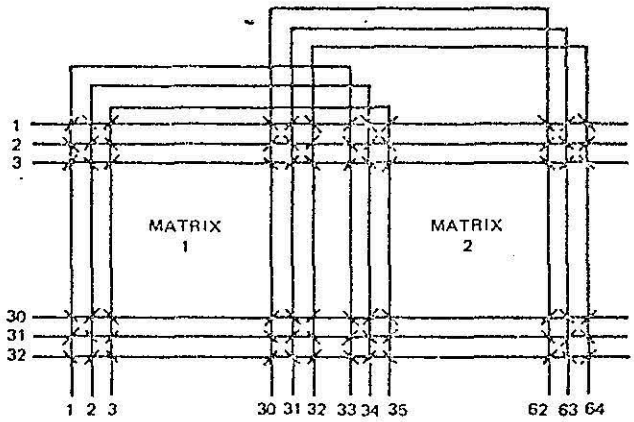

Fig. 31 2048-bit core array

The selected horizontal axis line provides half-select current for a string of cores. The selected vertical axis line supplies half-select current for two of the cores on the horizontal axis. Only one of the two cores, the selected core, has full select current flowing through it in the same direction. Refer to figure 32.

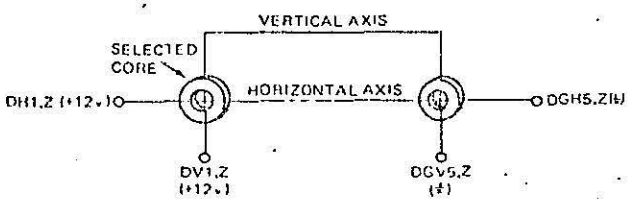

Fig. 32 Core selection

In addition to a horizontal axis line and a vertical axis line, each core has a sense wire running through it. This sense wire is connected to a sense amplifier supplying input to the memory latch.

SENSE AMPLIFIER

The memory sense winding runs through all of the cores in the array. The ends of the sense winding are connected through the windings of a pulse transformer to the inputs to a sense amplifier. The sense amplifier output, SA.C, is input to the memory latch.

The sense amplifier is used to determine when a ONE bit is read from the selected core. The sense amplifier only samples the sense winding voltage during the time CRU.GA is High. A further narrowing of the sampling window is provided by a strobe core and the associated strobe core sense amplifier.

Electrical noise within the memory core array is passed on to the sense winding. To reduce the effects of the noise, the

sense winding ends pass through the coils of the pulse transformer. The coils of the transformer, through mutual inductance, filter some of the noise.

To further reduce the effects of noise, a reference voltage of 20 millivolts must be exceeded before the sense amplifier recognizes the pulse on the sense windings as a bit.

STROBE CORE

The strobe core and its associated sense amplifier provide the fine timing for bit recognition. This core is identical to the cores used in the array. The current to change the state of this core is provided by the +12 v. supply during the read and write portions of each memory operation. Refer to figure 33.

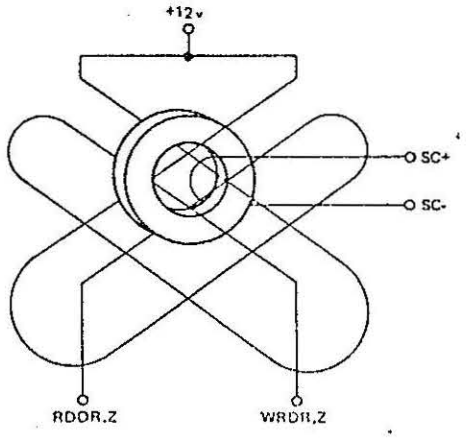

Fig. 33 Strobe core

The current drawn through the vertical axis lines is drawn through the strobe core. During the read portion of the memory operation, current for the activated vertical axis driver is drawn through the core on RDDR.Z. The core changes state inducing a pulse into the strobe core sense line, SC. If the pulse on SC exceeds 20 millivolts while CRU.GA is High, the strobe core sense amplifier outputs a timing pulse for the memory sense amplifier. The pulse is delayed 80 120 nsec. before being input to the memory sense amplifier.

During the write portion of memory operation, current is drawn through the strobe core in the opposite direction on WRDR.Z. The core then returns to the magnetic state it was in prior to reading. Although a pulse is induced into the SC line during this portion of the memory operation, the pulse is ignored because CRU.GA is Low during the write portion of a memory operation.

SUMMARY

The read/write memory module is designed to store variable data until the data is required by the control unit (TCU). The location of the data to be stored is determined by the TCU. The TCU also determines the data to be stored in the memory.

The process of accessing a character location and writing or reading data is essentially the same for either a read memory function or write memory function. In both functions, the memory module logic performs the same functions. Refer to figure 34.

In each read/write operation, the contents of the sector address register (C register) and character address register (A register) are decoded into a horizontal axis address and a vertical axis address. Included in the vertical axis address is the bit location within the selected character location.

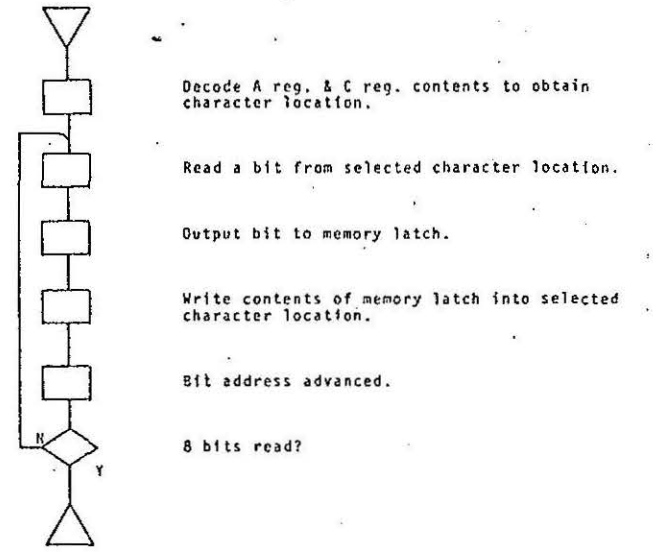

Fig. 34 Read/write flow

During the first half of each 7 μsec.bit time, the selected bit in the selected character is read. The state of the bit read is input to the memory latch, LATCH.L, if the function being performed is a read function. In the event that the function being performed is a write function, the bit read is ignored. In the read function, this portion of bit time is referred to as the read portion; in the write function this portion is referred to as the clear portion.

If a write function is being performed, the memory latch is loaded during the clear portion with the bit to be written.

During the second half of the bit time, the content of the memory latch is written into the selected bit position within the selected character. This portion of the bit time is referred to as the restore portion of a read function execution and the write portion of a write function execution.

The read/restore or clear/write cycles are repeated for each of the eight bits within the character. After the eighth bit is written or restored, the memory module logic remains static until the control unit accesses the module again.

The logic involved in performing the read/restore or clear/write operations for the first bit of character 000 of sector 0 is shown in figure 35.

After decoding the A-register and C-register contents, CBX.G goes High to activate the driver for DH1.Z (Q1) and the grounder for DGH5.Z (Q4). The current flow in the horizontal axis line during the read portion of the cycle is shown by the solid arrow.

Approximately 1.15 μsec. after the horizontal axis line is selected, CRU.GA comes High. CRU.GA activates the driver for DV1.G (Q5) and the grounder for DGV5.Z (Q8). The current for the vertical axis line during the read portion

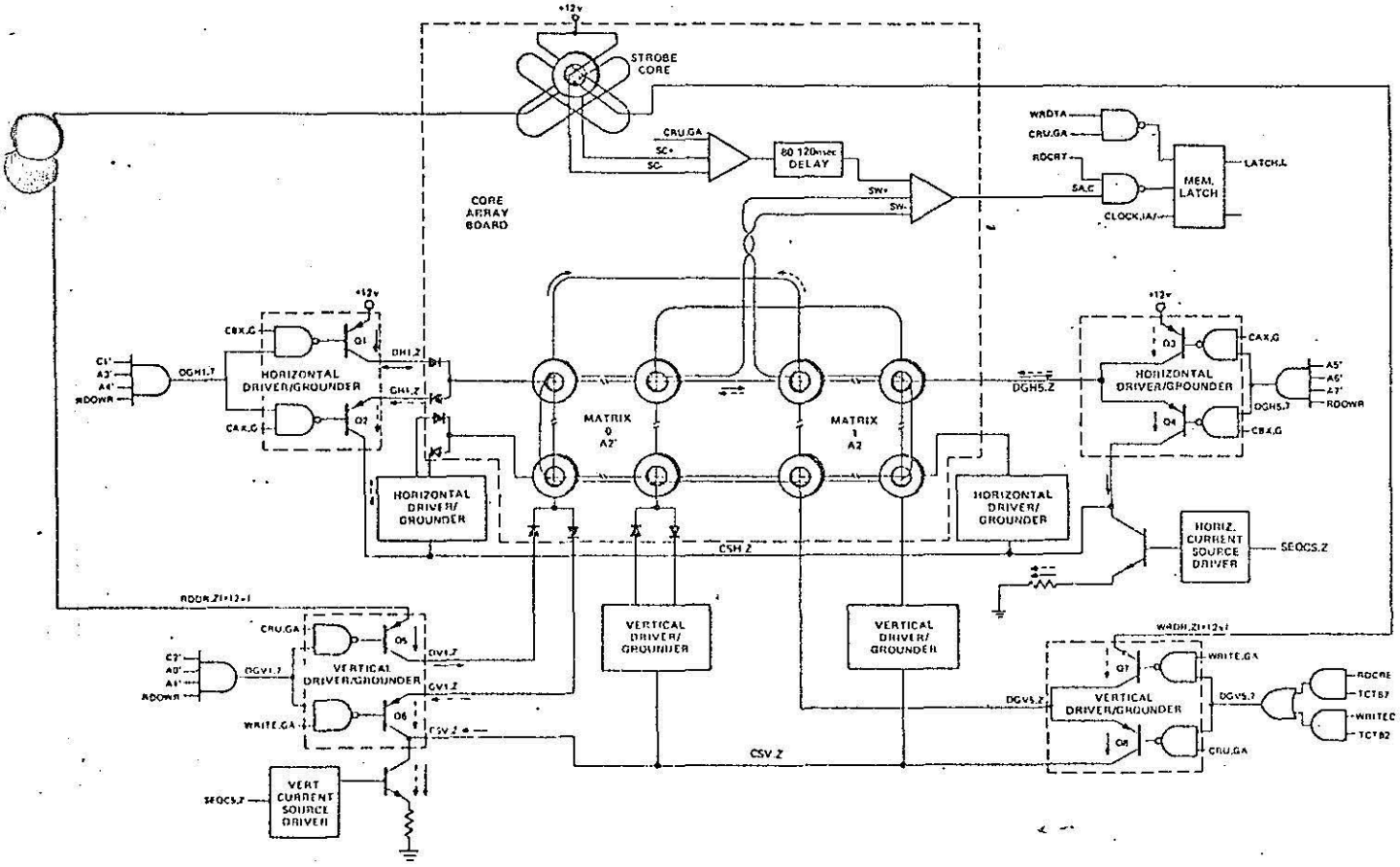

Fig. 35 Read/write logic

of the cycle (shown by solid arrow) is drawn from the +12 v. supply through the strobe core, the driver, the grounder, and to ground through the vertical axis current source.

The combined effect of the current in the horizontal and vertical axis changes the state of one core if the core was previously magnetized in the ONE state. Changing the magnetic state of the selected core induces a pulse in the sense winding (SW+, SW-). The pulse on the sense winding is input to the memory sense amplifier.

Timing, to ensure that the pulse on the sense winding is the output of the core read, is supplied by CRU.GA from the basic memory timing circuitry and by a pulse induced into the strobe core sense winding when vertical axis read current is drawn through the strobe core. Eighty to 120 nsec after the strobe core sense winding pulse is detected, the memory sense winding is sampled by the memory sense amplifier.

The output of the sense amplifier (SA.C) is input to the memory latch (LATCH.L) if a read memory function is being performed. If a write function is being performed, the memory latch is set to the state of the bit input to the module logic from the TCU.

During the second half of the read/write cycle, the timing term, WRITE.GA, is raised for 1.15 μsec. WRITE.GA High to the vertical axis driver/grounder activates the grounder or GV1.Z (Q6) and the driver for DGV5.Z (Q7). The current for the write portion of the cycle is supplied from the +12v. supply through the strobe core, the driver, the grounder, and the vertical axis line (shown by the broken arrow). This current restores the strobe core to its preread state.

If the memory latch is reset at the time WRITE.GA is generated, the horizontal axis timing term CAX.G remains Low and no horizontal axis current flows. CAX.G is High when WRITE.GA is generated for character location 000. CAX.G High activates the horizontal axis grounder (Q2) for GH1.Z and the driver (Q3) DGH5.Z. With current in both the horizontal and vertical axis lines, a ONE bit is written into the selected core in the selected character. The read/restore or clear/write cycles, as described in the preceding example, are performed for each read function or write function issued by the control unit (TCU).

QUESTIONS

1. Name the different models of M-17 memory and the variations among the models.
2. Name the seven function codes issued to the M-17 and give a brief description of each function.
3. What two types of data are transferred from the memory to the TCU?
4. What feature of the M-17 memory modules prevents the loss of stored data during power upsequencing or downsequencing?
5. Name the function of each bit of the character address register.

TEST POINTS	M-17-1-STD	M-17-2-280	M-17-3-STD
TP1	+12v.d.c. (RDDR.Z*)	+12v.d.c. (RDDR.Z*)	+12v.d.c. (WRDR.Z*)
TP2	+12v.d.c. (WRDR.Z*)	+12v.d.c. (WRDR.Z*)	+12v.d.c. (RDDR.Z*)
TP3	+ Strobe core Sense amp. input	+ Strobe core sense amp. input	-5.1v.d.c. sense amp. bias
TP4	- Strobe core sense amp. input	- Strobe core sense amp. input	+ Strobe core sense amp. input
TP5	20 millivolt sense amp. reference	20 millivolt sense amp. reference	- Strobe core sense amp. input
TP6	+ Sense winding sense amp. input	- Sense winding sense amp. input	Strobe core sense amp. output
TP7	- Sense winding sense amp. input	+ Sense winding sense amp. input	20 millivolt sense amp. reference
TP8	Strobe core sense amp. output	Strobe core sense amp. output	Delayed strobe core sense amp. output
TP9	Delayed strobe core sense amp. output	Delayed strobe core sense amp. output	+ Sense winding sense amp. input
TP10	-5.1v.d.c. sense amp. bias	-5.1v.d.c. sense amp. bias	- Sense winding sense amp. input

Table 5 M-17 test points

SERVICE INFORMATION

Test points are provided on the core array board of each model of M-17 memory. The test points, listed in table 5, can be used as an aid in isolating a malfunction to the core array board. For additional troubleshooting aids, refer to the technical information handbook or manual for the unit containing the M-17 module.

ANSWERS

1. Name the different models of M-17 memory and the variations among the models.

   The three models of the M-17 memory are M-17-1-STD, M-17-2-280, and M-17-3-STD. The memories vary in size from 2K (M-17-1-STD) to 4K (M-17-2-280) to 8K (M-17-3-STD).

2. Name the seven function codes issued to the M-17 and give a brief description of each function.

   a. Receive Sector Address — The receive sector address is issued to prepare the memory to accept the two-bit sector address. The sector address selects one of a possible four 2048-bit memory sectors.

   b. Receive Character Address — Receipt of the receive character address function prepares the memory to accept an eight-bit binary address to be stored in the character address register. The character address is decoded to select the horizontal and vertical lines through the core array.

   c. Present Character Address — The memory module transfers the eight-bit contents of the character address register to the TCU after receiving this function.

   d. Read Memory — After receiving the read memory function, the memory module reads the data stored in the character location specified by the contents of the sector address register and the character address register. The eight data bits read are transferred to the TCU.

   e. Write Memory — The memory module stores the eight-bit data character received following the write memory function in the character location specified by the contents of the sector address and character address registers.

   f. Advance Character Address/Read Memory — After receiving this function, the memory module increments the contents of the character address register and reads the data from the location specified by the contents of the sector address register and incremented character address register. The eight-bit data character read is transferred to the TCU.

   g. Advance Character Address/Read Memory/Write Memory — This function is the same as the advance character address/read memory function except that, following the reading of the character, the TCU transfers a data character to the memory. This character is stored in the location specified by the contents of the sector address register and incremented character address register.

3. What two types of data are transferred from the memory to the TCU?

   The contents of the character address register is transferred to the TCU after receiving a present character address function. The data read from memory is transferred to the TCU during execution of a read memory, advance character address/read memory, or advance character address/read memory/write memory function.

4. What feature of the M-17 memory modules prevents the loss of stored data during power upsequencing or downsequencing?

   The sequence control circuit prevents the operation of the current sources if the +12 v.d.c. supply output is below +9 v.d.c. When the current sources are inoperable, the state of the cores cannot be changed.

5. Name the function of each bit of the character address register.

   The five most significant bits (A_3 through A_7) of the character address register are used in selecting the vertical lines. Bit A_2 selects the matrix containing the desired character location. Bits A_0 and A_1 are used in the selection of a vertical line through the core array.